AN INTEGRATED BIPOLAR TRANSMITTER FOR DECT

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Abstract

An integrated bipolar transmitter IC for DECT is presented. The influence of the open loop architecture commonly used for the DECT system on the TX-IC concept is discussed in detail. It is shown that a two chip radio can achieve a higher integration level than a single chip solution.

Introduction

The Digital Enhanced Cordless Telecommunication system (DECT) has a strong demand for highly integrated RF-ICs due to the main application in the consumer market. The transmitter IC presented here is part of a second generation chip set (Fig. 1) [1] which has been designed to achieve a low cost DECT radio. Low cost means from this point of view not just to integrate as much as possible into one IC or to target a single chip transceiver. The major target is to reduce the overall bill of material including external passive and active components, specially expensive RF-components.

DECT System requirements

DECT is a TDMA system using 12 receive (RX) and 12 transmit (TX) time slots within a 10 ms frame. Moreover there are 10 channels available between 1880 MHz and 1900 MHz. A GFSK modulation with a bit rate of 1.152 Mbits/s is used. GFSK is basically GMSK at B·T=0.5, allowing for large tolerances in order to make the implementation simple. Due to this an open loop modulation is commonly used, i.e. an active transmit slot is always preceded by a so called blind slot. Obviously this will result in a reduced traffic capacity of the radio, because only 6 of the possible 12 connections can be handled. Nevertheless a mobile part needs a maximum of two connections in order to initiate a hand over. For most fixed part appli-

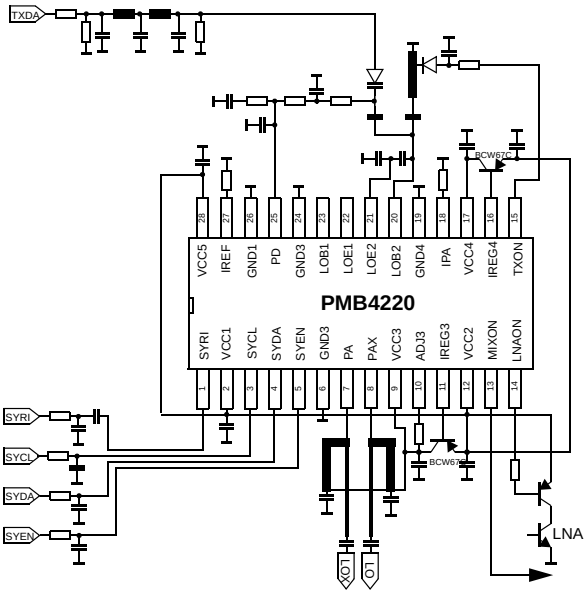

Figure 2: Application circuit.

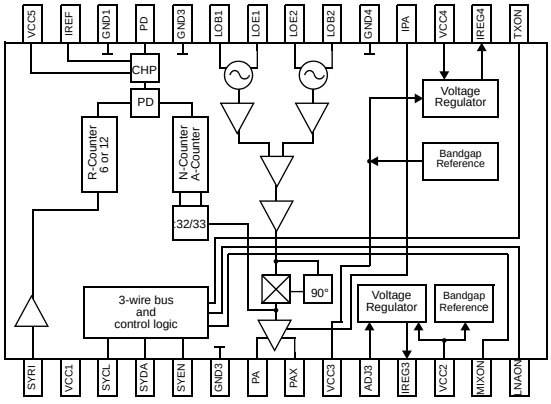

Figure 3: Pin configuration.

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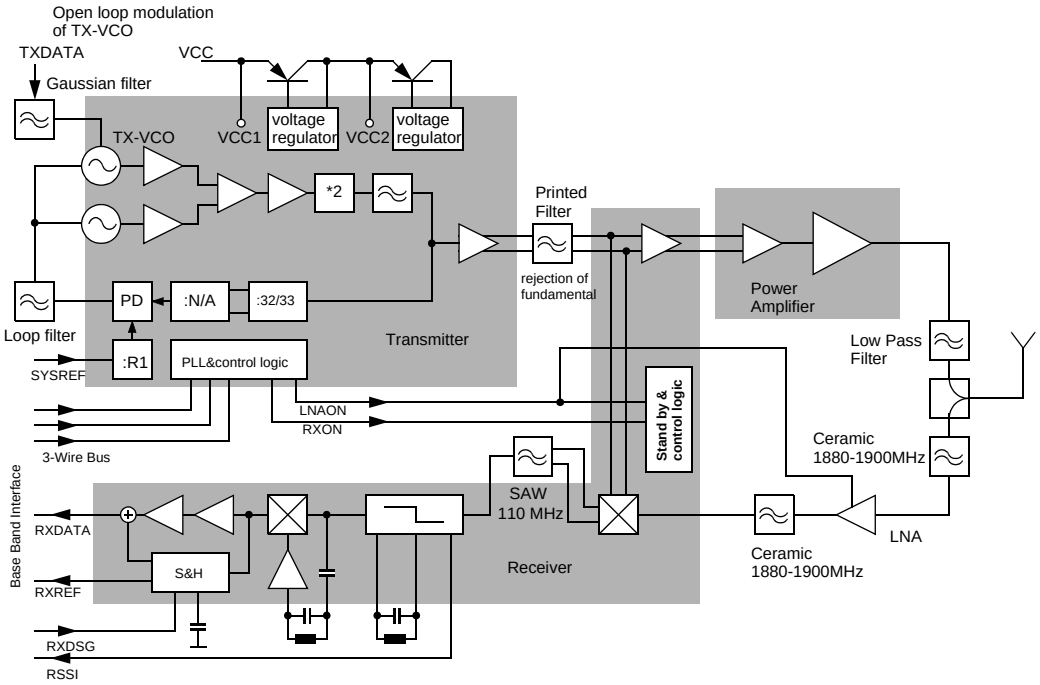

Figure 1: DECT radio block diagram of the 2nd generation chip set.

cations 6 connections are sufficient. Only the fixed part in applications like PABX or last mile with high traffic density have a demand for a zero blind slot radio.

Implementation

The blind slot radio architecture enables the use of the open loop modulation concept in the transmit path. This results in a very simple TX-architecture, which is the equivalent to the homodyn architecture in the RX case. During the blind slot the synthesizer can settle down to the desired channel. At the beginning of the active transmit slot the charge pump is switched into stand by mode forcing the loop to be opened. The VCO is then simply modulated by supplying the gaussian filtered binary data to the varactor diode, which has already been used for channel adjustment (cf. Fig. 2). The major problem of this approach is to achieve a stable output frequency. As shown in Fig. 1, the IC has to generate the LO-signal for the single conversion receiver. Due to the high IF of 110 MHz it is difficult to use a single VCO to synthesize both RX and TX frequencies within a single band. Therefore the IC (refer to Fig. 3) supports either a two VCO approach, where one VCO is used for RX and the other for TX, or a two band solution as indicated in Fig. 2. In a real DECT radio there are a lot of factors, which have a negative influence on the frequency stability. First there is the radiation from the antenna. Only shielding

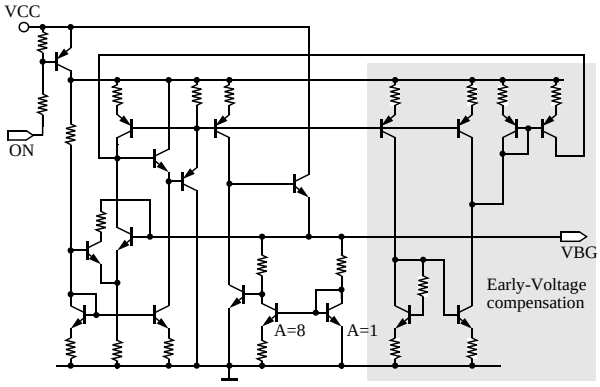

Figure 4: Schematic of the bandgap reference circuit.

helps and this can not be targeted from the IC design point of view. The second major problem is the supply voltage. The commonly used two cell supply concept with a DC/DC converter results in a 100 kHz, 200 mV ripple on the supply. Moreover, the converters current driving capabilities are low, resulting in a supply voltage drop of 300 mV up to 500 mV if the power amplifier is switched on. Under these circumstances, the 1st generation chip set needed a lot of additional external supply decoupling in order to obtain the required frequency stability [2]. There are two possible solutions to overcome this problem. The VCO could be realized completely off chip in order to achieve the im-

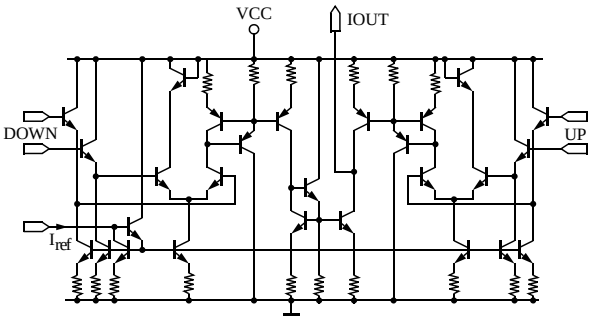

Figure 5: Schematic of the charge pump circuit.

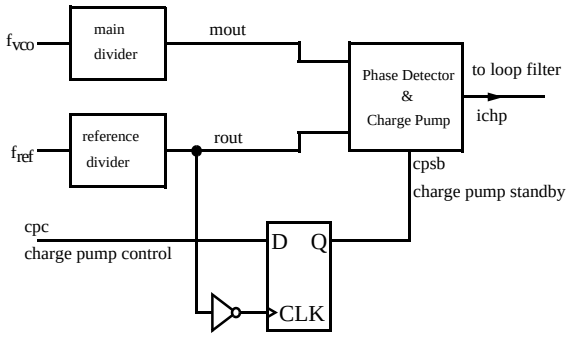

Figure 6: Simplified block diagram of the open loop switching synchronization.

provement by external decoupling. This approach results in an increased component count and a higher bill of material mainly due to the VCO RF-BJT. In the presented IC an additional second low drop voltage regulator is integrated. Therefore only an external low cost PNP BJT is needed to increase the overall ripple rejection to about 80 dB. Due to the superior performance of the 25 GHz bipolar process used for implementation the overall supply voltage of 3.0 V has been maintained by reducing the VCO supply to 2.2 V. Moreover, supply ripple rejection of the bandgap reference has been increased by a new Early-voltage compensation (Fig. 4). The compensation technique increases the ripple rejection of each bandgap reference by 20 dB, supplying the sensitive analog part of the chip with highly stable bias currents.

The next problem is the load pulling caused by switching on the power amplifier. A single chip implementation would require external discrete buffers isolating the VCO from the input impedance variation of the power amplifier, because the package does not give the required isolation. Running the VCO at half the output frequency and using internal frequency doubling in combination with a carefull choice of the pin configuration (Fig. 3) is not sufficient, even if the VCO is realized externally. This problem is

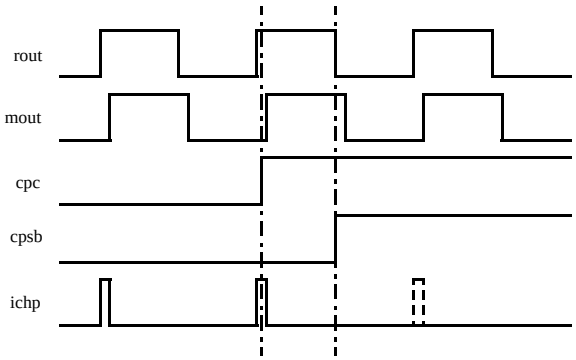

Figure 7: Simplified timing diagram of open loop switching synchronization.

one of the major reasons for choosing a two chip implementation, because the isolation could be provided by the package of the RX IC as shown in Fig. 1. As indicated a completly differential setup is used to achieve at least 30 dB of isolation with an optimized layout of the PCB. The last major problem of the open loop concept from the IC design point of view is the mechanism of opening the loop. In the first generation [2] the switching point was set by a micro controller using the lock detect output of the general purpose synthesizer causing additional complexity. In the new implementation the synthesizer has been optimized for DECT resulting in short programming words. At the beginning of the blind slot after power up 12 bits are sent for frequency and setup information. At the beginning of the active slot 3 bits are send to control the charge pump standby and the RX control outputs. Refering to Fig. 5, the 3-wire bus enable signal controlls the stand by switching of the charge pump. In order to guarantee that the charge pump will not be switched while a current is flowing, the switching is delayed to the falling edge of the reference divider output. Due to the even ratio of the reference divider a 50% duty cycle can be guaranteed. A simplified block diagram as well as a timing diagram are given in Fig. 6 and Fig. 7, respectively. The phase detector acts on the rising edge, therefore only a few nA will be left at the point of switching. This results in the behavior shown in Fig. 8.

There is actually no frequency offset due to the stand by mode of the charge pump. Another reason for the excellent behavior is that just the UP and DOWN inputs of the charge pump are switched to inactive, whereas the bias current is maintained.

Therefore, no switching transient occurs. Only a small disturbance due to the 3-wire bus programming has been observed. A first DECT radio demonstrator has already proven the TX IC as well as the chip set concept. The frequency variation due to all the discussed problems has

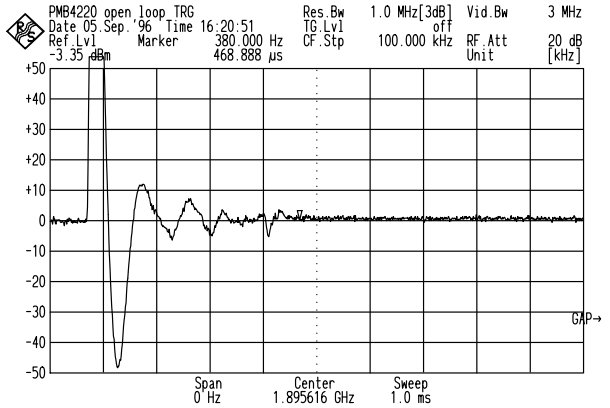

Figure 8: Open loop switching behavior.

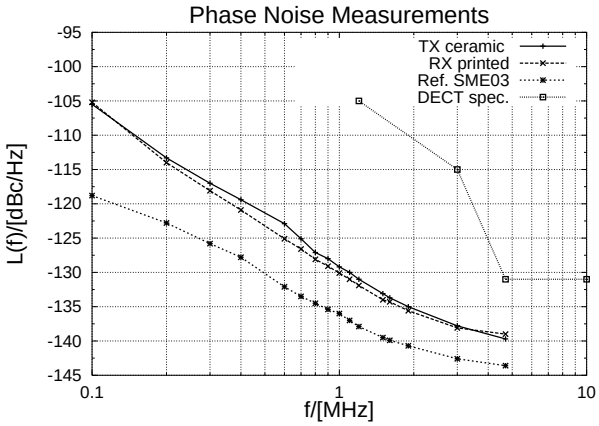

Figure 9: Phase noise measurement results.

been typically about 2 KHz compared to 50 kHz DECT system requirement. During the open loop mode leakage currents within the loop filter or the charge pump output would result in a frequency slope. Due to the blind slot concept, the loop bandwidth can be reduced yielding in a single loop filter capacitor of 10 nF. This high capacitance value is desirable in order to tolerate possible leakage currents. As shown in Fig. 8 the slope is about 200 Hz/ms, which is very low compared to the DECT requirement of 13 kHz/ms.

The phase noise performance requirements of the DECT system are determined by the specification of the unwanted emissions due to modulation. In the first and second adjacent channel the emmissions are dominated by the contribution of the modulation itself and can be fullfilled easily. The major requirement is to achieve a phase noise floor of a least -131 dBc/Hz within the 3rd and higher adjacent channels. The VCOs are realized as single ended Colpitts oscillators with an integrated active part, an external resonator and a tuning diode (Fig. 2). Compared to the first generation using ceramic resonators the performance has been increased by about 3 dB to -139 dBc/Hz at 4.7 MHz offset, whereas now printed and ceramic resonators give nearly the same performance. It should be noted that the measurement curves given in Fig. 9 are already approaching the accuray limits of the spectrum analyser used. Therefore, the measurment results of a Rhode&Schwarz signal generator has been included in order show that measurement is limited by the equipment. Anyway, -139 dBc/Hz gives already a margin of 8 dB to the DECT requirement.

Conclusions

Based on the presented transmitter IC a DECT complaint open loop radio can be implemented. It has been shown that for the DECT open loop concept a two chip implementation (excluding the power amplifier) is the best way to reduce the cost of the overall radio by achieving a high integration level, especially from the RF point of view.

References

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[2] S. Heinen, S. Beyer, and J. Fenk. “A.3.0V 2GHz Transmitter for Digital Radio Communication with integrated VCOs,” *1995 IEEE Int. Solid-State Circuits Conf.*, pp. 146-147, 1995.